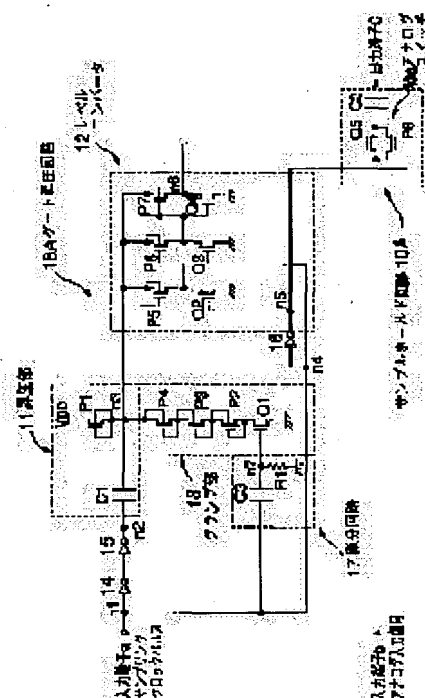


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**SOLUTION:** This semiconductor device has an A/D converter including a sample-and-hold circuit 10A and a gate boosting circuit 18A which boosts the gate voltage of an analog switch 10a included in the sample holding circuit 10A. The gate boosting circuit 18A has a boosting part 11 which boosts a sampling clock pulse controlling the analog switch 10a, a clamp circuit 13 which supplies a current to the ground to prevent the sampling clock pulse from being boosted above a specific value, and a differentiating circuit 17 which operates the clamp part 13 only the moment the sampling clock pulse goes up to a high level.



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